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1400 V 4H-SiC Power MOSFETs

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Abstract

Silicon Carbide (4H-SiC), power U-Metal-Oxide-Semiconductor Field-Effect Transistors (UMOSFETs) were fabricated and characterized from room temperature to 200°C. The devices had a 12 μm thick lightly doped n-type drift layer, and a nominal channel length of 4 μm. When tested under Fluorinert™ at room temperature, blocking voltages ranged from 1.3 kV to 1.4 kV. Effective channel mobility ranged from 1.5 $cm^2/V{\cdot}s$ at room temperature with a gate bias of 32 V (oxide field ~ 3.5 MV/cm) up to 7 $cm^2/V{\cdot}s$ at 100°C with an applied gate bias of 26 V (oxide field ~ 2.9 MV/cm). Specific on-resistance ($R_{on,sp}$) was calculated to be as low as 74 $m\Omega{\cdot}cm^2$ at 100°C under the same gate bias. Fowler-Nordheim measurements with positive gate bias on actual UMOS devices indicated thermionic field injection at elevated temperatures.

Introduction

SiC power Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), as compared to Si power MOSFETs, offer a potential for 10-20x lower on-resistance for the same die size (beneficial for lower conduction losses) or 10-20x smaller die size for the same on-resistance (beneficial for higher frequency operation or lower switching losses at the same frequency). These advantages are a direct result of 4H-SiC's high electric breakdown strength (2.2 MV/cm). While the advantages of SiC power MOSFETs have been long known, processing issues [1-3] have prevented these devices from reaching commercial systems thus far. Recent work on the Double-Implanted Metal-Oxide-Semiconductor (DIMOS) devices have demonstrated 760 V breakdown and a low specific on-resistance, $R_{on,sp}$, of 66 $m\Omega.cm^2$ at an applied gate bias of 30 V (~ 6.25 MV/cm) [4], while other lower voltage (260 V) SiC UMOSFETs have reported extremely low on-resistance of 18 $m\Omega{\cdot}cm^2$ [1] at an applied gate bias of 22 V (gate oxide thickness unreported). Most silicon carbide MOS devices posses low blocking voltages because of high-temperature and high electric field stress on the gate oxides. Additional problems with the UMOS structure in SiC include poor oxide uniformity, higher interface state densities on the sidewall, electric field crowding at the trench corners, and Fowler-Nordheim carrier injection across the gate oxide as a result of lower barrier heights for electron injection in the (4H-SiC)-SiO_2-polysilicon system [3,5]. Despite the technical challenges, the UMOS structure still offers inherent advantages over the DIMOS structure including smaller pitch and lower potential $R_{on,sp}$ due to the absence of the JFET region. Here, we report on a SiC UMOSFET capable of blocking up to 1.4 kV using a 12 μm thick drift layer.

Device Design and Fabrication

A cross-section of the 4H-SiC UMOSFET fabricated is shown in Fig. 1(a). A top view photograph of a 4H-SiC UMOS (13 μm pitch between fingers) is shown in Fig. 1(b), with gate and

source/body contacts shown. The device structure was grown by vapor phase epitaxy on a heavily doped n-type, Si-face, 8° off-axis, 4H-SiC substrate. The 12 μm thick drift layer was doped with nitrogen (n-type) at ~ 2 x 10^{15} cm^{-3} as verified from capacitance-voltage measurements. Next, the p-type channel layer (N_A ~ 7 x 10^{16} cm^{-3}) was grown for a nominal channel length (L) of 4 μm. An orthogonal source and body contact was formed by implanting the n^+ source regions in channel layer and then implanting a p^+ region between the source regions. Sintered nickel ohmic contacts were used for the drain and source/body. A common final metal connected source and body together, again, (see Fig. 1b), with a top layer of gold used to facilitate gold-gold wirebonding. The gate trench and edge termination were both accomplished via reactive ion etching in CHF_3, H_2, and O_2. Extensive organic and chemical cleans [6,7], as well as UV ozone cleaning to remove graphitic carbon from the surface, were performed prior to gate oxidation. A sacrificial oxide was grown prior to actual gate oxidation to smooth the trench corners (reduce field crowding) as well as consume damaged surface layers created by RIE. To minimize the difference in oxidation rates between the bottom and sides of the trench, the gate oxidation was done by growing a thin layer of thermal SiO_2 at 1150°C in steam, followed by a low pressure chemical vapor deposition of SiO_2 to obtain a more uniform gate oxide approximately 90 nm thick. After gate oxidation, polysilicon gates were deposited and selectively patterned to form the gate contact. Boron (p-type) doping of the polysilicon gate was used to reduce Fowler-Nordheim tunneling through the gate oxide [5]. Interdigitated source and gate fingers were of equal lengths (250 μm). The pitch varied from 13 to 38 μm, with smaller pitches preferred to minimize field crowding (for higher blocking voltage [8]). The number of fingers ranged from 10 to 40 for the different cells. No edge termination techniques were employed in these devices.

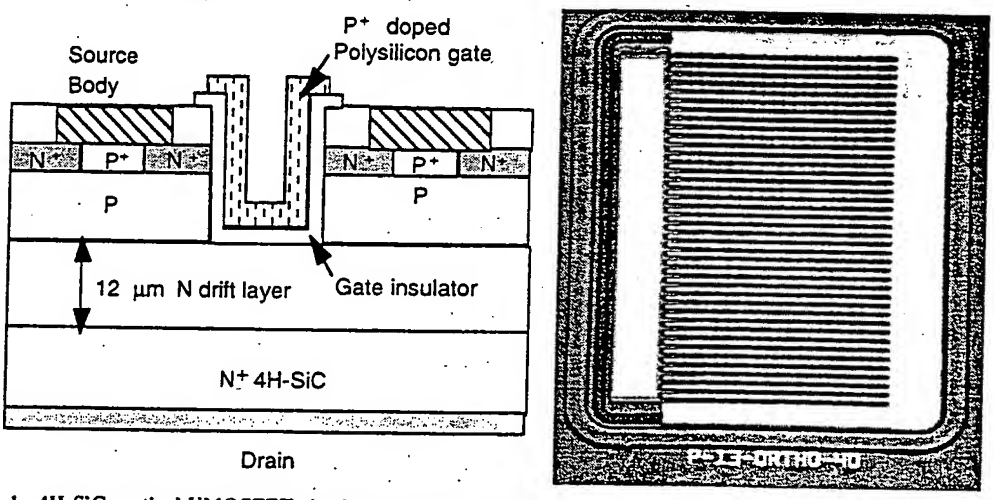

Fig. 1 4H-SiC vertical UMOSFET a) schematic device cross-section and b) top-view of a 13 μm pitch, 40 finger UMOS cell. Gate and source/body fingers shown with backside drain not shown. Gate length (L) was ~ 4 μm and trench width (W) was 20 mm.

Experimental Results and Discussion

Testing was performed on a high-temperature probe station in an air ambient with Fluorinert™. Specific contact resistivities were measured using TLM structures. Analysis of the n-type ohmic source data revealed a specific ohmic contact resistance of ~ 5-7 x10^{-6} Ω•cm^2, while the p-type body contact had a specific ohmic contact resistance of ~ 2-20 x10^{-3} Ω•cm^2.

Blocking voltages were measured from 1.3 to 1.4 kV. High-voltage forward I-V characteristics of a 1.4 kV SiC UMOS (13 μm pitch, 10 fingers) are shown in Fig. 2(a). The effective electron channel mobility was low, consistent with that reported in other SiC power MOS devices [1]. Values extracted from the linear region I-V characteristics of a typical device ranged from 1.5 $cm^2/V•s$ at room temperature with moderate applied gate bias (32 V or 3.5 MV/cm) and increased to 7 $cm^2/V•s$ at 100°C under 26 V (2.9 MV/cm) gate bias. The increase in inversion layer electron mobility with temperature is attributed to increased charge in the inversion layer as a result of electron emission from deeper level interface states, which has been reported elsewhere [7]. With V_{GS} of 26 V at 100°C, this device had a forward voltage drop of 8.0 V at a current density of 108 A/cm^2, which is shown in Fig. 2(b). The corresponding $R_{on,sp}$ was 74 $m\Omega•cm^2$ at this forward drop. While better performance could be obtained by increasing the gate bias (oxide field ~ 6-10 MV/cm), these values would exceed the practical operating limit of gate bias for SiO_2 on SiC [3,5].

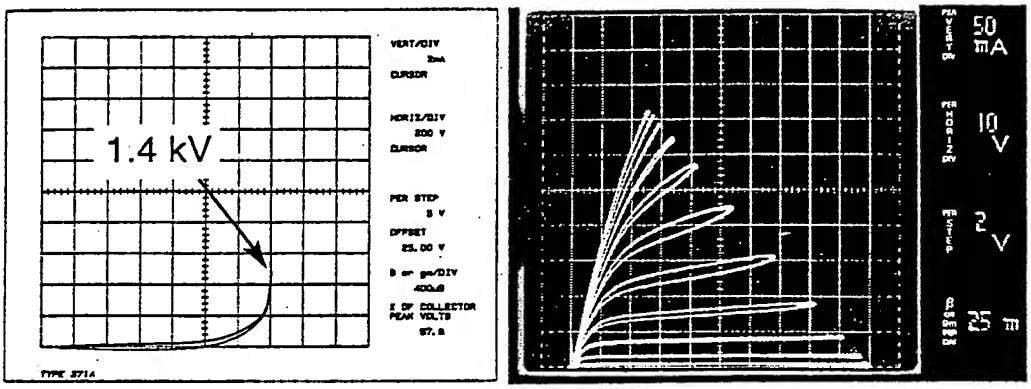

Fig. 2 (a) 4H-SiC UMOS blocking 1.4kV at room temperature under Fluorinert, (b) Low voltage I-V family of a 4H-SiC UMOSFET at 100°C, W = 20 mm, L = 4 μm, and t_{ox} = 900Å. First trace corresponds to V_{GS} of 6 V, incremented in 2 V steps to a maximum V_{GS} of 26 V (2.9 MV/cm) with $R_{on,sp}$ of 74 $m\Omega•cm^2$.

Due to the smaller barrier heights for electron injection from the SiC conduction band into the silicon dioxide conduction band as compared to Si (Fig. 3a), the time dependent dielectric breakdown (TDDB) and hot electron injection are expected to be serious reliability issues, especially if high temperature (>200°C) operation is considered - under on-condition. Fig. 3(b) shows the destructive IV plots for the actual UMOSFETs at different temperatures. The decrease in breakdown field of the gate dielectric with temperature is noted. This raises serious concerns about the reliability of SiC power MOS devices operating at elevated temperatures. In order to determine a maximum limit on the electric field across the gate oxide in 4H-SiC MOS system, long term TDDB measurements are needed. However, it is clear that the maximum electric field in the 4H-SiC MOS system should be much lower than the value used for silicon. It should be reduced further for operation at higher junction temperatures.

Conclusions

4H-SiC UMOSFETs have been fabricated and characterized with measured room-temperature blocking voltages ranging from 1.3 kV to 1.4 kV as a result of proper device design and fabrication, including the use of stacked grown/deposited gate dielectric, boron-doped polysilicon for gate contact, and common source/body contacts used to reduce the finger pitch. Reducing the finger pitch of the cells increased the charge sharing between fingers allowing for higher breakdown

voltage. Increasing the channel mobility (from 1.5 $cm^2/V\bullet s$ at room temperature and 7 $cm^2/V\bullet s$ at 100°C) by optimizing the SiC-SiO_2 interface was identified as a key task necessary to achieve optimal specific on-resistance. $R_{on,sp}$ was 74 $m\Omega\bullet cm^2$ with an applied gate bias of 2.9 MV/cm at 100°C for these devices.

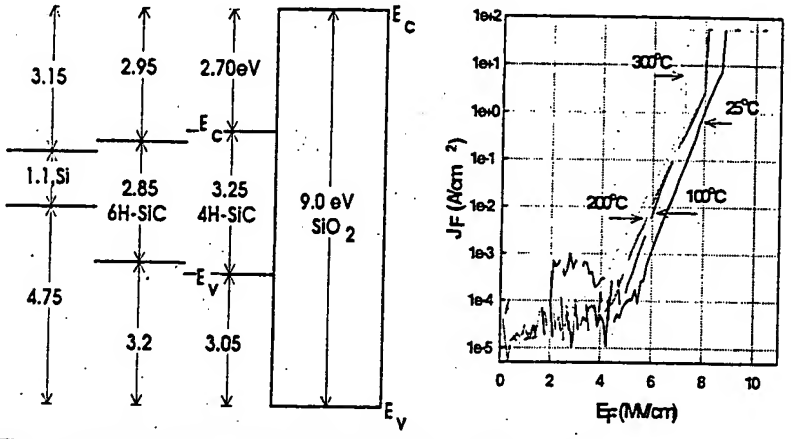

Fig. 3 (a) The energy band offsets of 6H-SiC and 4H-SiC wrt SiO_2, (b) Electron injection studies under positive gate bias on UMOSFETs with source and drain terminals at ground potential. The barrier for electron injection from 4H-SiC into SiO_2 conduction band is significantly lower than silicon.

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References

[1] J.W. Palmour, R. Singh, L.A. Lipkin, and D.G. Waltz, Trans. 3rd Int'l. Conf. on High Temperature Electronics (HiTEC), Albuquerque, NM, Vol. 2 (June 9-14, 1996), p. XVI-9.

[2] A.K. Agarwal, J.B. Casady, L.B. Rowland, W.F. Valek, and C.D. Brandt, submitted to IEEE Electron Device Lett. (1997).

[3] A.K. Agarwal, R.R. Siergiej, S. Seshadri, M.H. White, P.G. McMullin, A.A. Burk, L.B. Rowland, C.D. Brandt and R.H. Hopkins, Mater. Res. Soc. Symp. Proc., Vol. 423 (1996), p. 87.

[4] J.N. Shenoy, J.A. Cooper, Jr., and M.R. Melloch, IEEE Electron Device Lett., Vol. 18, No. 3 (1997), p. 93.

[5] A.K. Agarwal, S. Seshadri and L.B. Rowland, submitted to IEEE Electron Device Lett. (1997).

[6] J.N. Shenoy, G.L. Chindalore, M.R. Melloch and J.A. Cooper, Jr., J. Electron. Mater., Vol. 24, No. 4 (1995), p. 303.

[7] D.M. Brown, E. Downey, M. Ghezzo, J. Kretchmer, V. Krishnamurthy, W. Hennessy, and G. Michon, Solid-State Electron., Vol. 39, No. 11 (1996), p. 1531.

[8] Prof. T. Paul Chow, Rensselaer Polytechnic Institute, Troy, New York, private communication.